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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,927	08/03/2007	**Irwin Aberin**	1431.168.101/FIN 581 PCT/	9898

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EXAMINER	
JUNG, MICHAEL	

ART UNIT	PAPER NUMBER
2895	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,927	ABERIN ET AL.	
	Examiner	Art Unit	
	MICHAEL JUNG	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17,19-25,27-34 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,19-25,27-34 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/23/2009 has been entered.

In the submission, the Applicant cancelled claims 18, 26 and 35 and amended claims 17, 21-24, 30, 32 and 33 from the previous version of the claims (08/06/2009). Currently, claims 17, 19-25, 27-34 and 36 are pending.

Claim Objections

2. Claims 17, 19-25, 27-34 and 36 are objected to because of the following informalities:

For claim 17, please replace "its upper surface" and "its bottom surface" with --an upper surface of the substrate-- and --a bottom surface of the substrate--, respectively.

For claim 22, please delete "non-plated vent holes of" in the third line from the bottom of the claim, because it does not add further limit "the plurality of non-plated vent holes".

A limitation "the redistribution board" lacks antecedent basis. Please change the limitation to "the substrate".

For claim 24, please add --plurality of non-plated" before "vent holes at the upper surface in the last two lines of the claim.

For claim 30, please delete "non-plated vent holes of" in the third line from the bottom of the claim, because it does not add further limit "the plurality of non-plated vent holes".

For claim 33, please delete "each covered with a layer of solder resist" in line 2 as it conflicts with the last paragraph, in which the bottom surfaces are covered except in the contact areas.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 17, 19, 24, 25, 27-34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patent No. US 6,014,318 A to Takeda in view of Patent No. US 6,054,755 A to Takamichi et al. (hereinafter "Takamichi").

Regarding claim 17, Takamichi teaches a method comprising:

providing a substrate 1 comprising a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") and a plurality of upper conducting traces (Fig. 11 shows the "upper conducting traces" as sections of a third

wiring material layer (middle layer) of the five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring substrate..." (col. 6, ln 24-36")) and upper contact pads 12 (col. 6, ln 24-36) and upper contact pads 12 (col. 6, ln 24-36 - "a bump 12...is formed and the wiring substrate is connected to electrodes of the semiconductor chip.") on its upper surface (Fig. 11 shows a surface of the third wiring material layer (middle layer).), a second plurality of lower conductive traces 11 (Fig. 11 shows "lower conductive traces" as sections of the bottommost wiring material layer. Fig. 6 shows a bottommost material layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on its bottom surface and conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and lower conducing traces 11 (see Fig. 11);

forming a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") through the substrate 1 in a semiconductor chip 2 mounting area defined on the upper surface (Fig. 11 shows two vapor holes situated directly underneath the chip 2.) and in areas of the substrate adjacent to the semiconductor chip mounting area (Fig. 11 shows a vapor hole formed in an area to the left of the mounting area and another vapor hole formed in an area to the right of the mounting area.); and

covering the lower surface of the substrate 1 with a layer of solder resist 5 (col. 5, ln 53-55), but leaving the contact areas 10 free from solder resist 5 (see Fig. 11).

Takeda does not disclose a method of covering the upper surface of the substrate with a layer of solder resist.

However, Takamichi teaches a method of covering an upper surface of a substrate 21 (col. 4, ln 8-10) with a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Takeda with the method of covering the upper surface of the substrate with the layer of solder resist as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

The modified method as taught by the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Regarding claim 19, Takeda further teaches the vent holes 7 that include solder resist 5 (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist...").

Regarding claim 24, Takeda teaches a substrate 1 (col. 6, ln 4-11) for a semiconductor package (see Fig. 11) comprising:

a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material");

a plurality of upper conducting traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring

substrate..." (col. 6, ln 24-36")) and upper contact pads 12 (col. 6, ln 24-36) on an upper surface of the sheet (Fig. 11 shows a surface of the third wiring material layer (middle layer).), a second plurality of lower conductive traces (Fig. 11 shows "lower conductive traces" as sections of the bottommost wiring material layer. Fig. 6 shows a bottommost wiring layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on a bottom surface of the sheet and a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and lower conducing traces 11 (see Fig. 11);

a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") through the sheet in the semiconductor chip mounting area (Fig. 11 shows two vapor holes situated directly underneath the chip 2.) and in the areas of the substrate adjacent to the semiconductor chip mounting area (Fig. 11 shows a vapor hole formed in an area to the left of the mounting area and another vapor hole formed in an area to the right of the mounting area.); and

a layer of solder resist 5 (col. 5, ln 53-55) covering the lower surfaces of the substrate 1 (see Fig. 11), but leaving the contact areas 10 free from solder resist 5.

Takeda does not disclose a layer of solder resist covering the upper surface of the substrate.

However, Takamichi teaches a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C) covering an upper surface of a substrate 21 (col. 4, ln 8-10).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate of Takeda with the layer of solder resist covering the

upper surface of the substrate as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

The modified substrate as taught by the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Regarding claim 25, Takeda further teaches the vent holes 7 that include solder resist (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist...").

Regarding claim 27, Takeda further teaches the plurality of vent holes that are laterally located towards the center of the substrate (Fig. 11 shows two vapor holes situated directly underneath the center of the semiconductor chip 2.).

Regarding claim 28, Takeda further teaches the plurality of vent holes that are laterally located towards the center (Fig. 11 shows two vapor holes situated directly underneath the center of the semiconductor chip 2.) and towards the outer edges of the substrate (Fig. 11 shows a vapor hole formed in an area to the left of the mounting area and another vapor hole formed in an area to the right of the mounting area.).

Regarding claim 29, Takeda does not specifically disclose a diameter of the vent hole.

However, Takamichi teaches the vent holes each having a diameter ranging between 0.15 and 0.5 mm (col. 4, ln 23-24).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the diameter of the vent holes of Takeda to range between 0.15 and 0.5 mm as taught by Takamichi, so as to allow moisture produced during the reflow heating to escape the semiconductor package through the vent holes to prevent delamination (Takamichi, col. 5, ln 14-22).

Regarding claim 30, Takeda teaches a semiconductor package (see Fig. 11) comprising:

a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material");

a plurality of upper conducting traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring substrate..." (col. 6, ln 24-36")) and upper contact pads 12 (col. 6, ln 24-36) on an upper surface of the sheet (Fig. 11 shows a surface of the third wiring material layer (middle layer).), a second plurality of lower conductive traces (Fig. 11 shows "lower conductive traces" as sections of the bottommost material layer. Fig. 6 shows a bottommost material layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on a bottom surface of the sheet and a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and lower conducing traces 11 (see Fig. 11);

a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") through the sheet (see Fig. 11);

a layer of solder resist 5 (col. 5, ln 53-55) covering the lower surfaces of the sheet (see Fig. 11), but leaving the contact areas 10 free from solder resist 5; and

a semiconductor chip 2 including an active surface (Fig. 11 shows a surface facing the sheet 1) with a plurality of chip contact areas (col. 6, ln 33-34 - "electrodes of the semiconductor chip") electrically connected to the sheet 1, wherein non-plated vent holes 7 of the plurality of non-plated vent holes are disposed in an area of the sheet below the semiconductor chip 2 (Fig. 11 shows two vapor holes situated directly underneath the center of the semiconductor chip 2.) and in areas of the sheet adjacent to the semiconductor chip (Fig. 11 shows a vapor hole formed in an area to the left of the mounting area and another vapor hole formed in an area to the right of the mounting area.).

Takeda does not disclose a layer of solder resist covering the upper surface of the substrate.

However, Takamichi teaches a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C) covering an upper surface of a substrate 21 (col. 4, ln 8-10).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate of Takeda with the layer of solder resist covering the upper surface of the substrate as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

The modified substrate as taught by the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Regarding claim 31, Takeda further teaches the chip 2 that is encapsulated by mold material 3 (col. 6, ln 36-41; see Fig. 11).

Regarding claim 32, Takeda further teaches the chip 2 that is mounted to the sheet 1 by flip-chip technique (see Fig. 11).

Regarding claim 33, Takeda teaches a substrate 1 for a semiconductor package (Fig. 11) comprising:

a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") with an upper surface and a bottom surface, the bottom surface covered with a layer of solder resist 5 (see Fig. 11);

a plurality of upper conducting traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring substrate..." (col. 6, ln 24-36")); and upper contact pads 12 (col. 6, ln 24-36) on the upper surface (Fig. 11 shows a surface of the third wiring material layer (middle layer).),

a second plurality of bottom conductive traces (Fig. 11 shows "lower conductive traces" as section of the bottommost wiring material layer. Fig. 6 shows a bottommost wiring layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on the bottom surface;

a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and bottom conducing traces 11 (see Fig. 11);

a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") through the sheet in a chip mounting area defined on the upper surface (Fig. 11 shows two vapor holes situated directly underneath the chip 2.) and in areas adjacent to the chip mounting area (Fig. 11 shows a vapor hole formed in an area to the left of the mounting area and another vapor hole formed in an area to the right of the mounting area.); and

a layer of solder resist 5 (col. 5, ln 53-55) covering the bottom surfaces of the substrate (see Fig. 11), but leaving the contact areas 10 free from solder resist 5.

Takeda does not disclose a layer of solder resist covering the upper surface of the substrate.

However, Takamichi teaches a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C) covering an upper surface of a substrate 21 (col. 4, ln 8-10).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate of Takeda with the layer of solder resist covering the upper surface of the substrate as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

The modified substrate as taught by the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Regarding claim 34, Takeda further teaches the vent holes 7 that include solder resist (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist...").

Regarding claim 36, Takeda further teaches the plurality of vent holes that are laterally located towards the center of the substrate (Fig. 11 shows two vapor holes situated directly underneath the center of the semiconductor chip 2.).

4. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda and Takamichi, and further in view of Pub. No. US 2001/0042908 A1 to Okada et al. (hereinafter "Okada").

Regarding claim 20, neither Takeda nor Takamichi discloses the vent holes that are formed by drilling.

However, Okada teaches forming vent holes 16 by drilling (para [0052]).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide for vent holes of Takeda by drilling as taught by Okada as a matter of design choice in light of Okada's teaching that vent holes can be formed by punching (para [0052]), lasing (para [0064]) and drilling (para [0052]).

Regarding claim 21, neither Takeda nor Takamichi discloses forming the vent holes in the core material before forming a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and depositing conducting vias.

However, Okada teaches forming vent holes 16 in the core material 6 before a plurality of upper contact traces and upper contact pads on its surface, a second

plurality of lower conducting traces and external contact areas on its bottom surface and depositing conducting vias (para [0052] - "...the semiconductor device shown in Fig. 5 has a plurality of vent holes (through holes) 16 previously formed in an organic substrate 6...").

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Takeda with forming the vent holes in the core material before forming contact traces, contact pads, external contact areas and conducting vias as taught by Okada, in order to simply the method of assembling a semiconductor package by not having to form the vent holes after forming contact and conducting features.

5. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda and Takamichi, and further in view of Pub. No. 2002/0043721 A1 to Weber et al. (hereinafter "Weber").

Regarding claim 22, the combination of Takeda and Takamichi teaches a method comprising:

providing a substrate 1 comprising a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") and a plurality of upper contact traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of the five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring substrate..." (col. 6, ln 24-36")) and upper contact pads 12 (col. 6, ln 24-26) on its upper surface (see Fig. 11), a second

plurality of lower conducting traces 11 (Fig. 11 shows "lower conductive traces" as sections of the bottommost wiring material layer. Fig. 6 shows a bottommost material layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "ball electrode terminal 10") on its bottom surface and conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and lower conducting traces 11 (see Fig. 11);

forming a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") in the substrate 1;

covering the lower surface of the substrate 1 with a layer of solder resist 5 (col. 5, ln 53-55), but leaving the contact areas 10 free from solder resist 5 (see Fig. 11);

providing a semiconductor chip 2 comprising an active surface (Fig. 11 shows a surface facing the sheet 1) including a plurality of chip contact areas 9col. 6, ln 33-34 - "electrodes of the semiconductor chip");

mounting the chip 2 on the upper surface of the substrate 1 by microscopic solder balls 12 (col. 6, ln 32-33 - "a bump 12 using solder") between the chip contacts and upper contact areas, wherein non-plated vent holes 7 of the plurality of non-plated vent holes 7 are disposed in an area of the substrate below the semiconductor chip (Fig. 11 shows two vapor holes situated directly underneath the center of the semiconductor chip 2.) and in area adjacent to the semiconductor chip (Fig. 11 shows a vapor hole formed in an area to the left of the mounting area and another vapor hole formed in an area to the right of the mounting area.); and

underfilling the area between the chip 2 and the upper surface of a redistribution board 1 with epoxy resin 3 (col. 6, ln 36-41; see Fig. 11).

Takeda does not disclose a method of covering the upper surface of the substrate with a layer of solder resist.

However, Takamichi teaches a method of covering an upper surface of a substrate 21 (col. 4, ln 8-10) with a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Takeda with the method of covering the upper surface of the substrate with the layer of solder resist as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

The modified method as taught by the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Neither Takeda nor Takamichi discloses performing a solder reflow.

However, Weber teaches performing a solder reflow (para [0008]).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method as taught by the combination of Takeda and Takamichi with performing a solder reflow as taught by Weber, so as to electrically contact the semiconductor chip with circuit traces of the substrate (Weber, para [0008]).

Regarding claim 23, Takeda further teaches covering the upper surface of the chip 2 and the substrate1 with a mold material 3 (col. 6, ln 36-41; see Fig. 11).

Response to Arguments

6. Applicant's arguments with respect to claims 17, 19-25, 27-34 and 36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL JUNG whose telephone number is (571) 270-3345. The examiner can normally be reached on Mondays through Fridays from 8:30 AM to 6:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL JUNG/
Examiner, Art Unit 2895
21 January 2010

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895